Rockwell

R6500 Microcomputer System
DATA SHEET

RAM, I/O, INTERVAL TIMER DEVICE (RIOT)

DESCRIPTION

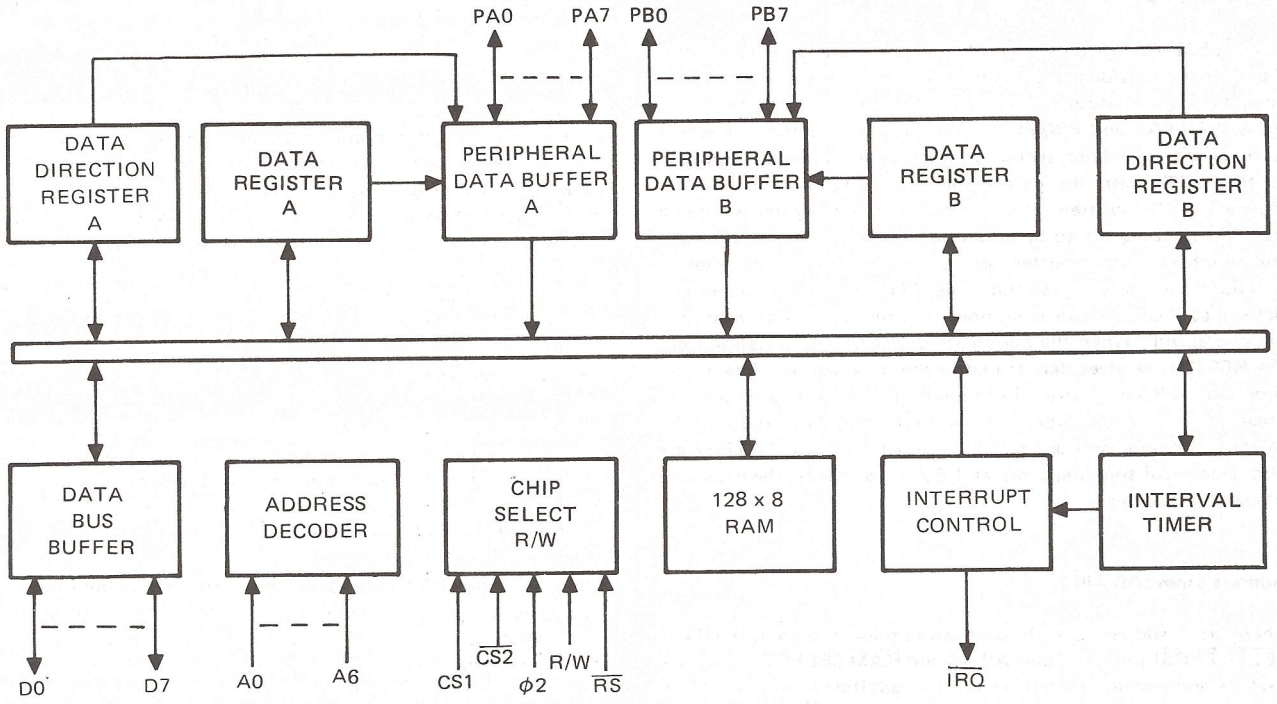
The R6532 is designed to operate in conjunction with the R6500 Microprocessor Family. It is comprised of a 128 x 8 static RAM, two software-controlled, 8-bit bidirectional data ports allowing direct interfacing between the microcomputer and peripheral devices, a software programmable interval timer with interrupt, capable of timing in various intervals from 1 to 262,144 clock periods, and a programmable edge-detect circuit.

FEATURES

- 8 bit bidirectional Data Bus
- 128 x 8 static RAM
- Two 8 bit bidirectional data ports
- Programmable Interval Timer with interrupt capability
- TTL & CMOS compatible peripheral lines
- One port has Direct Transistor Drive Capability
- Programmable edge-sensitive interrupt input
- 6500/6800 bus compatible
- 1 MHz and 2 MHz parts available

Ordering Information

Order Number	Package Type	Temperature Range	Frequency Range
R6532P	Plastic	0°C to +70°C	1 MHz
R6532C	Ceramic	0°C to +70°C	1 MHz
R6532PE	Plastic	-40°C to +85°C	1 MHz
R6532CE	Ceramic	-40°C to +85°C	1 MHz
R6532AP	Plastic	0°C to +70°C	2 MHz
R6532AC	Ceramic	0°C to +70°C	2 MHz



R6532 Block Diagram

Specifications subject to change without notice
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INTERFACE SIGNAL DESCRIPTION

Reset ($\overline{RES}$)

During system initialization a logic "0" on the $\overline{RES}$ input will cause a zeroing of all four I/O registers. This in turn will cause all I/O buses to act as inputs thus protecting external components from possible damage and erroneous data while the system is being configured under software control. The Data Bus Buffers are put into an OFF-STATE during Reset. Interrupt capability is disabled with the $\overline{RES}$ signal. The $\overline{RES}$ signal must be held low for at least two clock periods when reset is required.

Read/Write (R/W)

The R/W signal is supplied by the microprocessor and is used to control the transfer of data to and from the R6532. A high on the R/W pin allows the processor to read (with proper addressing) the data supplied by the R6532. A low on the R/W pin allows a write (with proper addressing) to the R6532.

Interrupt Request ($\overline{IRQ}$)

The $\overline{IRQ}$ pin is an interrupt pin from the interrupt control logic. The pin will be normally high with a low indicating an interrupt from the R6532. An external 3K pull-up resistor is required. The $\overline{IRQ}$ pin may be activated by a transition on PA7 or timeout of the interval timer.

Data Bus (D0-D7)

The R6532 has eight bidirectional data pins (D0-D7). These pins connect to the system's data lines and allow transfer of data to and from the microprocessor. The output buffers remain off or tri-stated except when the R6532 is selected for a Read operation.

I/O Ports (PA0-PA7, PB0-PB7)

The R6532 has 16 pins available for peripheral I/O operations. Each pin is individually software programmable to act as either an input or an output. The 16 pins are divided into two 8-bit ports, PA0-PA7 and PB0-PB7. (PA7 also has another use which is discussed in a later section.) Each is set up as an input by writing a "0" into the corresponding bit of the data direction register. A "1" written into the data direction register will cause its corresponding bit to be an output. When in the input mode, the peripheral output buffers are in the "1" state and the internal pull-up device acts as less than one TTL load to the peripheral data lines. On a Read operation, the microprocessor reads the peripheral pin. When the peripheral device gets information from the R6532 it receives data stored in the data register. The microprocessor will read correct information if the peripheral lines are greater than 2.0 volts for a "1" and less than 0.8 volt for a "0" as the peripheral pins are all TTL compatible. Pins PB0-PB7 are also capable of sourcing 3 ma at 1.5V, thus making them capable of Darlington drive.

Address Lines (A0-A6)

There are 7 address pins. In addition to these 7, there is the $\overline{RAM\ SELECT}$ ($\overline{RS}$) pin. The pins A0-A6 and $\overline{RAM\ SELECT}$ are always used as addressing pins. There are two additional pins which are used as CHIP SELECTS. They are pins CS1 and $\overline{CS2}$.

INTERNAL ORGANIZATION

The R6532 is divided into four basic sections, RAM, I/O, TIMER, and Interrupt Control. The RAM interfaces directly with the microprocessor through the system data bus and address lines. The I/O section consists of two 8-bit halves. Each half contains a Data Direction Register (DDR) and a Data Register (DR).

RAM – 128 Bytes (1024 Bits)

The 128 x 8 Read/Write Memory acts as a conventional static RAM and can be accessed from the microprocessor by selecting the chip (CS1 = 1, $\overline{CS2}$ = 0) and by setting $\overline{RS}$ to a logic 0 (0.4V). Address lines A0 through A6 are then used to select the desired byte of storage.

I/O Registers

The 'A' side I/O port consists of eight lines which can be individually programmed to act as either an input or an output. A logic zero in a bit of the Data Direction Register (DDRA) causes the corresponding line of the 'A' port to act as an input. A logic one causes the corresponding 'A' line to act as an output. The voltage on any line programmed to be an output is determined by the corresponding bit in the Data Register (DRA).

Data is read directly from the data pins during any read operation. For any output pin, the data transferred into the processor will be the same as that contained in the Data Register if the voltage on the pin is allowed to go to 2.4V for a logic one. Note that for input lines, the processor can write into the corresponding bit of the Data Register. This will not affect the polarity on the pin until the corresponding bit of DDRA is set to a logic one to allow the I/O line to act as an output.

The operation of the 'B' side Input/Output port is exactly the same as the normal I/O operation of the 'A' side port. Each of the eight lines can each be programmed to act as either an input or as an output by placing a 0 or a 1 into the Data Direction register (DDRB). In the output mode, the voltage on a peripheral pin is controlled by the Data Register (DRB).

The primary difference between the 'A' port and the 'B' port is in the operation of the output buffers which drive these pins. The 'B' side output buffers are push-pull devices which are capable of sourcing 3 ma at 1.5V. This allows these pins to directly drive transistor switches. To assure that the microprocessor will read proper data on a "Read 'B' side" operation, sufficient logic is provided in the chip to allow the microprocessor to read the Output Register instead of reading the peripheral pin as on the 'A' port.

Edge Detecting with PA7

In addition to acting as a peripheral I/O line, the PA7 line can be used as an edge-detecting input. In this mode, an active transition will set the internal interrupt flag (bit 6 of the Interrupt Flag register). Setting the interrupt flag will cause $\overline{IRQ}$ output to go low if the PA7 interrupt has been enabled.

Control of the PA7 edge detecting mode is accomplished by writing to one of four addresses. In this operation, A0 controls the polarity of the active transition and A1 acts to enable or disable interrupting of the processor. The data which is placed on the Data Bus during this operation is discarded and has no effect on the control of PA7.

The PA7 interrupt flag will be set on an active transition, even if the pin is being used as a normal input or as a peripheral control output. The flag will also be set by an active transition if the PA7 interrupt is disabled. The reset signal ($\overline{RES}$) will disable the PA7 interrupt and will set the active transition to negative (high-to-low). During the system initialization routine, it is possible to set the interrupt flag by a negative transition. It may also be set by changing the polarity of the active interrupt. It is therefore recommended that the interrupt flag be cleared before enabling interrupting from PA7. To clear the PA7 Interrupt Flag, simply read the Interrupt Flag Register.

Interval Timer

The Timer section of the R6532 contains three basic parts: preliminary divide down register, programmable 8-bit register and interrupt logic.

The interval timer can be programmed to count up to 255 time intervals. Each time interval can be either 1T, 8T, 64T or 1024T increments, where T is the system clock period. When a full count is reached, an interrupt flag is set to logic "1". After the interrupt flag is set the internal clock begins counting down at the system clock rate to a maximum of -255T. Thus, after the interrupt flag is set, a Read of the timer will tell how long since the flag was set up to a maximum of 255T.

The 8-bit system Data Bus is used to transfer data to and from the Interval Timer. If a count of 52 time intervals were to be counted, the pattern 0 0 1 1 0 1 0 0 would be put on the Data Bus and written into the divide by 1 Interval Timer register.

At the same time that data is being written to the Interval Timer, the counting intervals of 1, 8, 64, 1024T are decoded from address lines A0 and A1. During a Read or Write operation address line A3 controls the interrupt capability of PB7, i.e., A3 = 1 enables $\overline{IRQ}$, A3 = 0 disables $\overline{IRQ}$. When the timer is read prior to the interrupt flag being set, the number of time intervals remaining will be read, i.e., 51, 50, 49, etc.

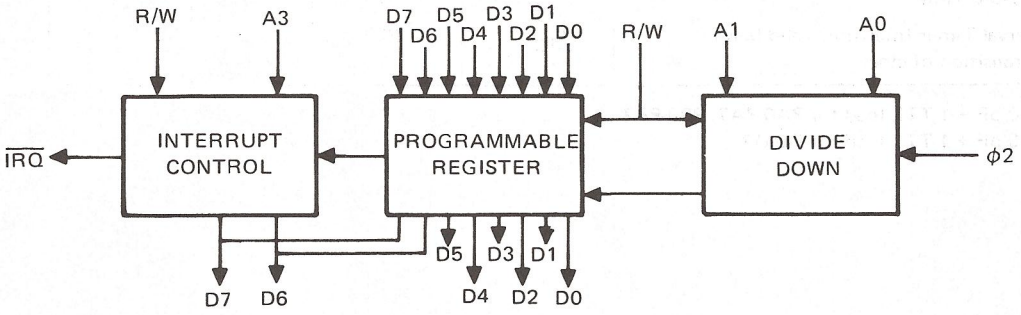
When the timer has counted thru 0 0 0 0 0 0 0 0 on the next count time an interrupt will occur and the counter will read 1 1 1 1 1 1 1 1. After the interrupt flag is set, the timer register decrements at a divide by "1" rate of the system clock. If the timer is read after the Interrupt Flag is set and a value of 1 1 1 0 0 1 0 0 is read, the time since interrupt is 27T. The value read is in two's complement, but remember that interrupt occurred on count number one. Therefore, we must subtract 1.

Value read	=	1 1 1 0 0 1 0 0	
Complement	=	0 0 0 1 1 0 1 1	
ADD 1	=	0 0 0 1 1 1 0 0	= 28 Equals two's complement of register
SUB 1	=	0 0 0 1 1 0 1 1	= 27

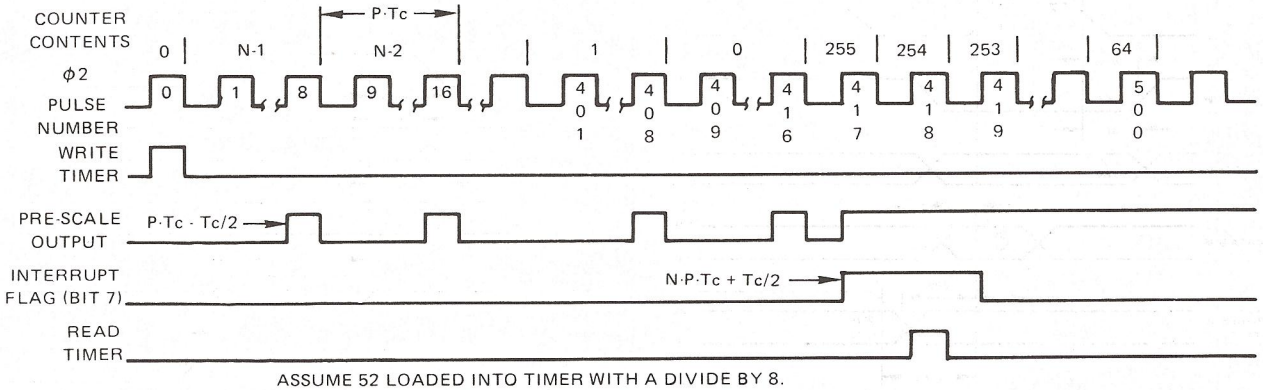
Thus, to arrive at the total elapsed time, merely do a two's complement add to the original time written into the timer. Again, assume time written as 0 0 1 1 0 1 0 0 (=52). With a divide by 8, total time to interrupt is (52 x 8) + 1 = 417T. Total elapsed time would be 416T + 27T = 443T, assuming the value read after interrupt was 1 1 1 0 0 1 0 0.

The interrupt flag will be reset whenever the Timer is accessed by a read or a write. However, the reading of the timer at the same time the interrupt occurs will not reset the interrupt flag. When the interrupt flags are read (D7 for the timer, D6 for the edge detect) data bus lines D0-D5 go to 0.

When reading the timer after an interrupt, A3 should be low so as to disable the $\overline{IRQ}$ pin. This is done so as to avoid future interrupts until after another Write timer operation.



Basic Elements of Interval Timer



ASSUME 52 LOADED INTO TIMER WITH A DIVIDE BY 8.
THE COUNTER CONTENTS AND THE CLOCK PULSE NUMBERS WILL COINCIDE.
Prescale, P = 8
Cycle Time, Tc = 1 μsec (for 1 MHz)
Count, N = 52

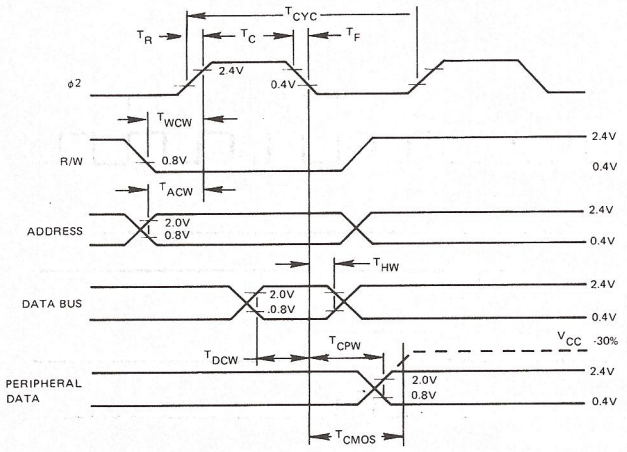
Write Timing Characteristics

Characteristic	Symbol	1 MHz		2 MHz		Unit
		Min	Max	Min	Max	
Clock Period	T_{CYC}	1	10	0.5	10	μs
Rise & Fall Times	T_R, T_F		25		25	ns
Clock Pulse Width	T_C	470		235		ns
R/W valid before positive transition of clock	T_{WCW}	180		90		ns
Address valid before positive transition of clock	T_{ACW}	180		90		ns
Data Bus valid before negative transition of clock	T_{DCW}	300		150		ns
Data Bus Hold Time	T_{HW}	10		10		ns
Peripheral data valid after negative transition of clock	T_{CPW}		1		0.5	μs
Peripheral data valid after negative transition of clock driving CMOS (Level = VCC – 30%)	T_{CMOS}		2		1	μs

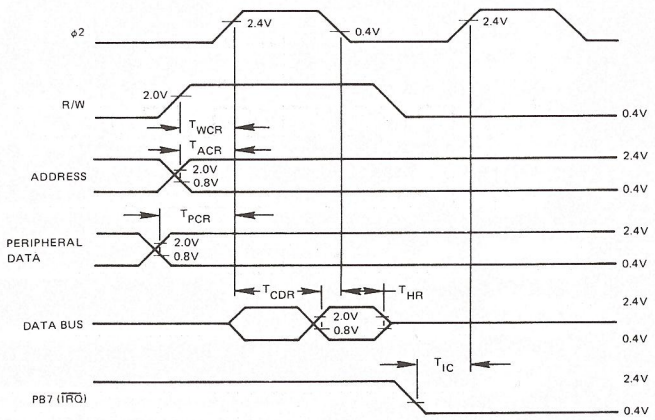
Read Timing Characteristics

Characteristic	Symbol	1 MHz		2 MHz		Unit
		Min	Max	Min	Max	
R/W valid before positive transition of clock	T_{WCR}	180		90		ns
Address valid before positive transition of clock	T_{ACR}	180		90		ns
Peripheral data valid before positive transition of clock	T_{PCR}	300		150		ns
Data Bus valid after positive transition of clock	T_{CDR}		395		190	ns
Data Bus Hold Time	T_{HR}	10		10		ns
IRQ (Interval Timer Interrupt) valid before positive transition of clock	T_{IC}	200		100		ns

Loading = 30 pF + 1 TTL load for PA0-PA7, PB0-PB7
= 130 pF + 1 TTL load for D0-D7



Write Timing Characteristics



Read Timing Characteristics

Address Decoding

Operation	$\overline{RS}$	R/W	A4	A3	A2	A1	A0
Write RAM	0	0	–	–	–	–	–
Read RAM	0	1	–	–	–	–	–
Write Output Reg A	1	0	–	–	0	0	0
Read Output Reg A	1	1	–	–	0	0	0
Write DDRA	1	0	–	–	0	0	1
Read DDRA	1	1	–	–	0	0	1
Write Output Reg B	1	0	–	–	0	1	0
Read Output Reg B	1	1	–	–	0	1	0
Write DDRB	1	0	–	–	0	1	1
Read DDRB	1	1	–	–	0	1	1
Write Timer							
÷1T	1	0	1	(a)	1	0	0
÷8T	1	0	1	(a)	1	0	1
÷64T	1	0	1	(a)	1	1	0
÷1024T	1	0	1	(a)	1	1	1
Read Timer	1	1	–	(a)	1	–	0
Read Interrupt Flag	1	1	–	–	1	–	1
Write Edge Detect Control	1	0	0	–	1	(b)	(c)

NOTES: – = Don't Care, "1" = High level (≥2.4V), "0" = Low level (≤0.4V)

(a) A3 = 0 to disable interrupt from timer to $\overline{IRQ}$
A3 = 1 to enable interrupt from timer to $\overline{IRQ}$

(b) A1 = 0 to disable interrupt from PA7 to $\overline{IRQ}$
A1 = 1 to enable interrupt from PA7 to $\overline{IRQ}$

(c) A0 = 0 for negative edge-detect
A0 = 1 for positive edge-detect

Register Addressing

Start Address +	Register/Function	Start Address +	Register/Function
$0	DRA ('A' side data register)	$7	Write edge-detect control (positive edge-detect, enable intrrupt)
$1	DDRA ('A' side data direction register)	$C	Read timer (enable interrupt)
$2	DRB ('B' side data register)	$14	Write timer (divide by 1, disable interrupt)
$3	DDRB ('B' side data direction register)	$15	Write timer (divide by 8, disable interrupt)
$4	Read timer (disable interrupt)	$16	Write timer (divide by 64, disable interrupt)
$4	Write edge-detect control (negative edge-detect, disable interrupt)	$17	Write timer (divide by 1024, disable interrupt)
$5	Read interrupt flag register (bit 7 = timer, bit 6 = PA7 edge-detect)	$1C	Write timer (divide by 1, enable interrupt)
$5	Write edge-detect control (positive edge-detect, disable intrrupt)	$1D	Write timer (divide by 8, enable interrupt)
$6	Write edge-detect control (negative edge-detect, enable interrupt)	$1E	Write timer (divide by 64, enable interrupt)
		$1F	Write timer (divide by 1024, enable interrupt)

SPECIFICATIONS

Maximum Ratings

Rating	Symbol	Value	Unit
Supply Voltage	V_{CC}	-0.3 to +7.0	Vdc
Input Voltage	V_{in}	-0.3 to +7.0	Vdc
Operating Temperature	T_A		°C
Commercial		0 to +70	
Industrial		-40 to +85	
Storage Temperature	T_{STG}	-55 to +150	°C

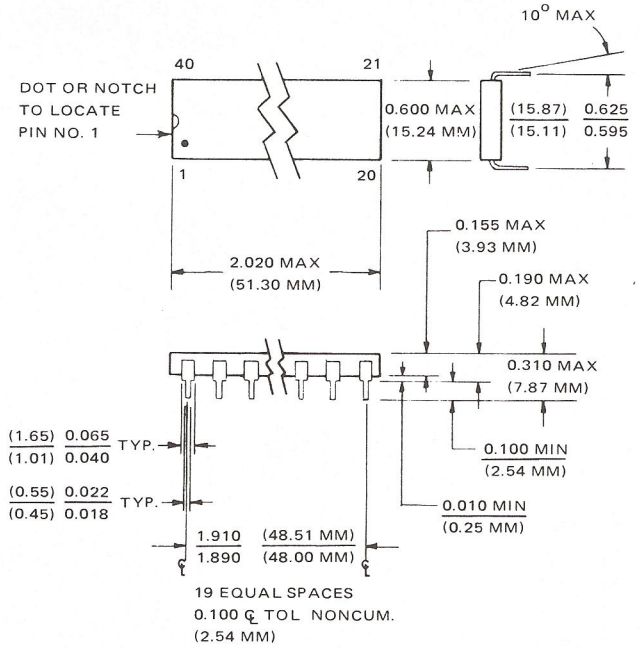
This device contains input protection against damage due to high static voltages or electric fields; however, precautions should be taken to avoid application of voltages higher than the maximum rating.

Electrical Characteristics

(V_{CC} = 5.0 ±5%, T_A = 0 - 70°C, Unless Otherwise Noted.)

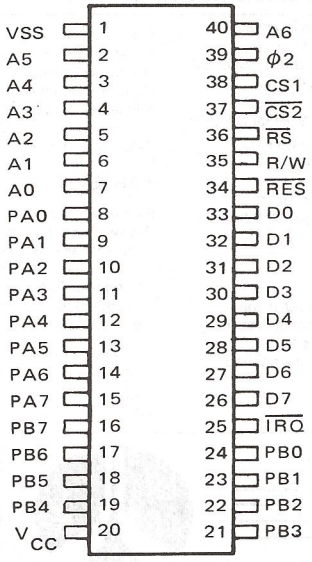
Characteristic	Symbol	Min	Typ	Max	Unit
Input High Voltage	V_{IH}	2.4	–	VCC	V
Input Low Voltage	V_{IL}	V_{SS}	–	0.4	V
Input Leakage Current: V_{IN} = +5.25V A0-A6, RS, R/W, $\overline{RES}$, ϕ2, CS1, $\overline{CS2}$	I_{IN}		–	2.5	μA
Input Leakage Current for High Impedance State (Three State): V_{IN} = 0.4V to 2.4V; D0-D7	I_{TSI}		– –	±10.0	μA
Input High Current: V_{IN} = 2.4V PA0-PA7, PB0-PB7	I_{IH}	-100	– –		μA
Input Low Current: V_{IN} = 0.4V PA0-PA7, PB0-PB7	I_{IL}		– –	-1.6	MA
Output High Voltage VCC = MIN, I_{LOAD} ≤-100 μA (PA0-PA7, PB0-PB7, D0-D7) I_{LOAD} ≤-3 MA (PB0-PB7)	V_{OH}	 2.4 1.5	 – –		V
Output Low Voltage VCC = MIN, I_{LOAD} ≤1.6 MA (D0-D7)	V_{OL}		–	0.4	V
Output High Current (Sourcing): VOH ≥2.4V (PA0-PA7, PB0-PB7, D0-D7) ≥1.5V Available for other than TTL (Darlingtons) (PB0-PB7)	I_{OH}	 -100 -3.0	 – –		 μA MA
Output Low Current (Sinking): VOL ≤0.4V (PA0-PA7) (PB0-PB7)	I_{OL}	1.6	–		MA
Clock Input Capacitance	C_{Clk}		–	30	pF
Input Capacitance	C_{IN}		–	10	pF
Output Capacitance	C_{OUT}		–	10	pF
Power Dissipation (T_A = 0°C)	P_D		500	1000	mW

All values are D.C. readings



NOTE: Pin No. 1 is in lower left corner when symbolization is in normal orientation

Packaging Diagram



Pin Configuration

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